In the Claims

Claims 1-96 cancelled.

97. (currently amended) A capacitor comprising:

a first capacitor electrode over a monocrystalline silicon substrate;

a second capacitor electrode;

a dielectric layer between the first and second capacitor electrodes; and

at least one of the first and second capacitor electrodes comprising hemispherical grain platinum formed by a process comprising:

flowing an oxidizing gas comprising O_2 at a flow rate of about 50 sccm into a reaction chamber;

flowing a platinum precursor comprising ~~MeCpPt(Pe)$_3$~~ MeCpPt(Me)$_3$ into the reaction chamber using carrier gas flowing through a bubbler at a pressure of about 6 Torr and a flow rate of about 5 sccm;

chemical vapor depositing hemispherical grain platinum from the platinum precursor over the substrate in the presence of the oxidizing gas, the hemispherical grain platinum having a continuous surface characterized by columnar pedestals; and

maintaining a temperature and pressure within the reaction chamber at about 215°C and 5 Torr, respectively, during the depositing.

98. (previously presented) The capacitor of claim 97 wherein the chemical vapor depositing occurs for about 6 minutes.

99. (previously presented) The capacitor of claim 97 wherein the carrier gas comprises He.

100. (previously presented) The capacitor of claim 97 wherein the first capacitor electrode comprises the hemispherical grain platinum.

101. (previously presented) The capacitor of claim 97 further comprising flowing at least one other metal precursor into the chamber in addition to the platinum precursor, and wherein the platinum is deposited as an alloy of platinum and the at least one other metal.

102. (previously presented) The capacitor of claim 97 wherein the hemispherical grain platinum comprises a platinum alloy comprising platinum and at least one of rhodium, ruthenium or palladium.

103. (previously presented) The capacitor of claim 97 wherein the oxidizing gas further comprises at least one of N_2O, SO_3, O_3, H_2O_2, and NO_x, wherein x has a value of from 1 to 3.

104. (previously presented) The capacitor of claim 97 wherein the platinum precursor further comprises at least one of $CpPtMe_3$, $Pt(acetylacetonate)_2$, $Pt(PF_3)_4$, $Pt(CO)_2Cl_2$, cis-$[PtMe_2(MeNC)_2]$, and platinum hexafluoroacetylacetonate.

105. (previously presented) The capacitor of claim 97 wherein the columnar pedestals have an average diameter of at least about 200 Å.

106. (previously presented) The capacitor of claim 97 wherein the columnar pedestals have an average diameter of about 200 Å.

107. (previously presented) The capacitor of claim 97 wherein the hemispherical grain platinum has a thickness of at least about 600Å.

108. (previously presented) The capacitor of claim 97 wherein the hemispherical grain platinum has a thickness of at least about 400Å, and less than about 1000Å.

109. (previously presented) The capacitor of claim 97 wherein the hemispherical grain platinum has a thickness of about 400Å or less.

110. (previously presented) An integrated circuit comprising:

a substrate;

a hemispherical grain platinum layer over the substrate, the hemispherical grain platinum layer having a continuous surface and characterized by columnar pedestals with an average diameter of at least about 200 Å; and

an intervening layer between the hemispherical grain platinum layer and the substrate.

111. (previously presented) The integrated circuit of claim 110 wherein the intervening layer comprises platinum.

112. (previously presented) The integrated circuit of claim 110 wherein the intervening layer comprises at least one of IrO_2, RuO_2, RhO_2, and OsO_2.

113. (previously presented) The integrated circuit of claim 110 wherein the substrate comprises monocrystalline silicon.

114. (previously presented) The integrated circuit of claim 110 wherein the hemispherical grain platinum layer is further characterized by columnar pedestals that are at least about 300Å tall.

115. (previously presented) The integrated circuit of claim 110 wherein the columnar pedestals have an average diameter of about 200 Å.

116. (previously presented) A capacitor comprising:

a first capacitor electrode over a monocrystalline silicon substrate;

a second capacitor electrode;

a dielectric layer between the first and second capacitor electrodes;

at least one of the first and second capacitor electrodes comprising hemispherical grain platinum having a continuous surface characterized by columnar pedestals having heights greater than or equal to about one-third of a total thickness of the platinum and having an average diameter of at least about 200 Å.

117. (currently amended) An integrated circuit comprising:

a semiconductive substrate;

a conductive node location disposed within the semiconductive substrate;

a first layer disposed over the semiconductive substrate and in electrical contact with the conductive node, the first layer comprising at least one of iridium, rhodium, ruthenium, palladium, osmium, silver, rhodium/platinum alloy, IrO_2, RuO_2, RhO_2, or OsO_2; and

a hemispherical grain platinum alloy layer disposed over the first layer, the platinum alloy layer characterized by a continuous outer surface, the platinum alloy layer comprising platinum and at least one of rhodium, iridium, ruthenium, palladium, osmium or silver, and the platinum alloy layer comprising columnar pedestal structures having heights greater than or equal to about one-third of a total thickness of the platinum alloy layer and having an average diameter of at least about 200 Å.

118. (previously presented) The integrated circuit of claim 117 wherein the platinum alloy layer comprises columnar pedestal structures having heights greater than or equal to about one-third of a total thickness of the platinum alloy layer.

119. (previously presented) The integrated circuit of claim 117 wherein the columnar pedestal structures have heights of at least 300Å.

120. (previously presented) The integrated circuit of claim 117 wherein the columnar pedestals have an average diameter of about 200 Å.